

APPLICATION FOR LETTERS PATENT
OF THE UNITED STATES

Roy C. Iggulden
Citizen of United States

Padraic Shafer
Citizen of United States

Werner Robl
Citizen of Germany

Kwong Hon Wong
Citizen of United States

TITLE OF INVENTION: LINER WITH POOR STEP COVERAGE TO IMPROVE
CONTACT RESISTANCE IN W CONTACTS

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION

**LINER WITH POOR STEP COVERAGE TO
IMPROVE CONTACT RESISTANCE IN W CONTACTS**

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BACKGROUND OF THE INVENTION

1. Field of the Invention

10 The present invention relates to the use of a liner
purposely having poor step coverage to improve the properties in
W vias. The liner is characterized by appropriate adhesion for
the W layer without increasing or widening the resistance values
and spread respectively.

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2. Description of The Prior Art

16 In general, semiconductors and integrated circuit devices
will comprise a silicon substrate and a doped region(s) disposed
in the semiconductor in which there are source or drain
connections, separated by a gate or gate control region. Metal
connections are made to the source, gate, and drain electrodes by
interconnects that are supported over the substrate by an
interlayer dielectric material.

20 Electrical connections are made between different layers by
patterning and etching the dielectric to form contact and via
openings. The openings are generally filled with electrically
conductive materials of plugs made of W (tungsten) that contact
previously doped regions, poly silicon or other metal layers. For
example, a layer of physical vapor deposited (PVD) metal such as
TiN is deposited in the sidewall of the contact/via openings to
support adhesion of the electrically conductive material or plug
of tungsten.

25 Since the ground rules or device geometry is getting
increasingly smaller and the contact/via aspect ratios are

5 becoming higher, step coverage of the TiN is becoming of increased concern because decreased step coverage requires the TiN layer to be thick enough to ensure sufficient deposition within a contact.

Further, in both single and dual damascene tungsten (W) interconnects contacting unlying metal layers, the contact resistance poses a problem because the W does not stick to oxide, thereby requiring the use of a liner to provide appropriate adhesion on the surface of the wafer; however, the problem is that the liner, which is generally made of TiN or a nitrogen treated Ti increases the contact resistance and also widens the resistance spread.

U.S. Patent 5,625,231 discloses a process for improving the structural and electrical integrity of contacts and interconnects comprising metals deposited by physical vapor deposition (PVD) or chemical vapor deposition (CVD) during processing of small ground rule semiconductor devices. The process entails: applying a TiN contact/via adhesion layer to a high aspect ratio contact/via opening etched in the dielectric by providing a first layer of TiN on the bottom of the contact/via opening and then depositing the second layer of TiN on the first layer of TiN and on the sidewalls of the contact/via opening. The second layer of TiN serves as the contact/via adhesion or glue layer.

A step coverage enhancement process for sub half micron contact/via is disclosed in U.S. Patent 5,654,233. The improved step coverage method for the sub-micron or sub-half-micron contact/via is obtained by using the conventional PVD TiN deposition process coupled with a selective reactive etching process which etches off only the overhang.

U.S. Patent 5,972,179 discloses a composite TiN barrier layer structure formed by depositing a first Ti layer by CVD to obtain good step coverage, followed by a second TiN layer formed

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5 by PVD to obtain uniform surface morphology for subsequent deposition of an aluminum alloy contact layer. By using a combination of these deposition techniques, with the last deposit made by PVD, the attributes of both deposition techniques are obtained, i.e. excellent step and bottom coverage characteristics
10 of the CVD technique, and uniform morphology characteristics of the PVD deposition technique.

U.S. Patent 5,654,589 discloses a process for forming multi layer interconnects that entails formation of Ti/TiN stack interconnect structures which may be used as local interconnects
15 and contact landing pads on the same level. The local interconnects and contact landing pads directly contact conductive regions of a semiconductor IC. The contact may be formed with previously doped regions in the semiconductor substrate, polysilicon, or other metal layers.

20 U.S. Patent 6,093,645 discloses a process for elimination of TiN film deposition in tungsten (W) plug technology using PECVD-Ti and in-situ plasma nitridation.

These patents improve the liner coverage to make sure the liner is covering all portions of the via. By doing this they fix
25 the adhesion that is brought about by the W/oxide interfaces.

In the art of semiconductors where single and dual damascene W interconnects contacting underlying metal layers, where contact resistance is a problem, because the W does not stick to oxide, and wherein a liner is utilized to provide appropriate adhesion
30 on the surface sidewall of the wafer, and wherein the liner (generally made of TiN or a nitrogen treated Ti) increases the contact resistance and also widens the resistance spread, there is a need for a liner that has very poor step coverage, that will coat the surface (to provide the necessary bulk adhesion for W)
35 but have little or no coverage at the via bottom and via

5 sidewalls so that there is improvements in via resistance and its spread.

The invention findings indicate that the vias themselves do not need to be coated with liner to achieve bulk adhesion.

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SUMMARY OF THE INVENTION

One object of the present invention is to provide, in the
15 case of a single damascene, where W interconnects contacting underlying metal layers and where the contact resistance is a problem, a liner with poor step coverage to improve the contact resistance in the W contacts.

Another object of the present invention is to provide, in
20 the case of a dual damascene, where W interconnects contacting underlying metal layers and wherein the contact resistance is a problem, a liner with poor step coverage to improve the contact resistance in the W contacts.

A further object of the present invention is to provide, in
25 the case of both single and dual damascene W interconnects contacting underlying metal layers and where the contact resistance is a problem because W does not stick to oxide and thereby requires a liner to secure adequate adhesion on the surface and sidewall of the wafer, a replacement of the
30 traditional liner with a liner of poor step coverage which will coat the surface but have no coverage at the via bottom.

A further object yet still of the present invention is to provide, in the case of both single and dual damascene W interconnects contacting underlying metal layers and where the
35 contact resistance is a problem because W does not stick to oxide and thereby requires a liner to secure adhesion to the surface

5 and sidewall of the wafer, a replacement of the traditional liner with a liner that decreases the contact resistance and lessens the resistance spread, through the use of a very poor step coverage PVD TiN coating, so that coating of the surface is provided without coverage at the via bottom.

10 These and other objects of the present invention will be more particularly described in the brief description of the drawings and detailed description of the preferred embodiments of the invention.

15 BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1a shows forming an interlevel dielectric layer and intermetal dielectric layer that is separated by an etch-stop layer on a semiconductor substrate in accordance with the invention.

FIG. 1b shows forming a line trench in the ILD layer of FIG. 1a.

FIG. 1c shows forming a very poor step coverage PVD TiN layer according to the invention.

FIG. 1d shows removal of the very poor step coverage PVD TiN layer, except from sidewalls of the line trench.

FIG. 3e shows forming a contact hole in the substrate of FIG. 1d.

FIG. 1f shows forming the dual damascene structure by tungsten (W) CVD deposition into the line trench and contact hole structure.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT OF THE INVENTION

5 The present invention is directed to fabricating and
manufacturing a current carrying metal filled contact/vias of
sub-micron diameter using a liner with poor step coverage to
improve the contact resistance in W contacts. The process can be
used in MOSFET or CMOS or any high density semiconductor device
10 presently being manufactured in the semiconductor industry;
however, only those specific areas unique to comprehension of
this invention will be described.

In general, a conductive plug filling a via hole is formed
by depositing an interlayer dielectric (ILD) on a conductive
15 layer comprising at least one conductive layer comprising at
least one conductive pattern, forming an opening through the ILD
by photolithographic and etching techniques, and filling the
opening with a conductive material. Excess conductive material on
the surface of the ILD is generally removed by chemical
20 mechanical polishing (CMP). One such method is known as the
single damascene technique and entails the formation of an
opening which is filled in with a metal.

Another such method is the dual damascene technique, which
involves the formation of an opening comprising a lower contact
25 or via hole section in communication with an upper trench
section, which opening is filled with a conductive material, such
as a tungsten, to simultaneously form a conductive plug in
electrical contact with a conductive line.

The invention process is accomplished by providing a
30 semiconductor substrate having active and passive regions;
forming an interlevel dielectric (ILD) layer over the substrate
having active and passive regions; forming an etch-stop layer
over the ILD layer; forming an intermetal dielectric (IMD) layer
over the etch-stop layer; forming a first photoresist layer over
35 the IMD layer and patterning the photoresist layer with a mask
comprising a line trench pattern; etching through the line trench

5 pattern in the first photoresist layer to form the line trench
 pattern into the IMD layer, wherein the line trench has a
 sidewall and a flat bottom; removing the first photoresist layer;
 forming a second photoresist layer over the IMD layer and and
 line trench having sidewalls; patterning the second photoresist
 10 layer with a mask comprising a contact hole pattern; etching
 through the contact hole pattern in the second photoresist layer
 to form a contact hole pattern into the interlevel dielectric
 (ILD) layer; removing the second photoresist layer; cleaning the
 contact hole; depositing a liner of very poor step coverage TiN
 15 by PVD in the line trench and the contact hole composite
 structure; and performing chemical mechanical polish to planarize
 the substrate for later process steps to finish fabrication of
 the semiconductor substrate.

Reference is now made to FIGS. 1a-f, where there is shown a
 20 dual damascene process using very poor step coverage PVD TiN to
 coat the surface but to basically provide no coverage of the via
 bottom. The process employs tungsten chemical vapor deposition
 for forming composite structures with local interconnects
 comprising line trenches with contact holes, and composite
 25 structures for intermetal interconnects with line trenches with
 via holes.

FIG. 1a shows a semiconductor substrate 10, with a
 substructure of devices formed therein; however, where they are
 not necessary to the invention, they will not be described in
 30 detail. The dual damascene process is applied in forming
 interconnects through via holes between metal layers. The method
 is applicable to both local interconnects with contact holes and
 to intermetal interconnects comprising via holes.

An interlevel dielectric (ILD) layer 11, is formed on
 35 substrate 10 of FIG. 1a. As is known, blanket dielectric layers
 may be formed from materials including silicon oxide materials,

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5 silicon nitride materials, and silicon oxynitrides materials
formed within integrated circuits through methods of CVD, PECVD,
PVD sputtering. In the invention, the blanket ILD layer is
preferably formed of silicon oxide. An etch-stop layer 12,
preferably of silicon nitride, is then formed over ILD layer 11.
10 The etch-stop layer serves to stop etching when the next layer is
etched to form line trenches.

The next layer of dielectric 13 in FIG. 1a is the intermetal
dielectric (IMD) layer formed above the ILD layer and below the
first metal layer that will be formed later. A phosphosilicate
15 glass (PSG), or, an oxide formed by the decomposition of
tetraethyl orthosilicate (TEOS) may be the IMD and is formed
using a plasma enhanced chemical vapor deposition (PECVD).

A first layer of photoresist (not shown) is formed over IMD
layer 13 and patterned with a mask having images of a line
20 trench.

Line trench 14 in FIG. 1b is formed by etching the line
trench pattern in the first photoresist layer into IMD layer 13
until etch-stop layer 12 is reached. Etching is accomplished
with a mixture comprising gases of O_2 , SO_2 and CF_4 . The etchant
25 is then modified to a mixture of gases O_2 , SO_2 , CF_4 and He so that
the etch-stop, silicon nitride layer 12, can be removed from the
bottom of trench 14 as shown in FIG. 1b. After removal of the
portion of etch-stop layer at the bottom of trench 14, the first
photoresist layer is removed.

30 The essential feature of the present invention is to next
introduce the step of providing a liner characterized by very
poor step coverage, such as PVD TiN to coat the surface but have
basically no coverage at the via bottom, as is shown in FIG. 1c.
In FIG. 1c TiN is deposited by physical vapor deposition (PVD)
35 and this PVD TiN layer 14 affects coverage of the sidewall 15 of

5 the via 16 and surface coats dielectric layer 13, but basically provides no coverage at the via bottom, as is shown in FIG. 1c.

The PVD TiN very poor step coverage layer 14 is next removed from the surface of the dielectric layer 13 but not the sidewalls 15 as shown in FIG. 1d. The removal is accomplished by using a
10 reactive ion etch which may comprise a mixture of SF₆, Hbr, and CCl₄. Alternatively, layer 14 may be removed using a CMP.

With layer 15 in place on the sidewalls of trench 16 a second layer of photoresist is formed over layer 11 and then patterned using a mask having images of a contact hole. As may
15 be seen from FIG. 1e, contact hole 17 is formed by etching the contact hole pattern in the second photoresist layer 13 until the surface of the substrate 10 is reached. The etching through the contact hole pattern in the second photoresist layer into the ILD layer may be accomplished using a gaseous mixture comprising
20 Ar, CHF₃ and C₄F₈. Following etching of the contact hole 17, the hole may optionally be cleaned by a well known technique such as sputtering.

As may be seen from FIG. 1e, the structure comprising line trench 15 and contact hole 17 collectively form the damascene
25 structure where the side-walls of the trench are covered with the very poor step coverage layer of PVD TiN, that basically provide no coverage at the via bottom.

The tungsten (W) interconnects contacting the underlying middle layers is next deposited into this damascene structure, as
30 shown in FIG. 1f. The tungsten interconnect 18 may be deposited using CVD by utilizing any well known process; however, exemplary of the process utilized to deposit the tungsten interconnect is that of silane reduction, as shown by the reaction in the following formula:

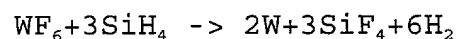


Table 1

Liner	Contact Resistance Range
IMP TI	4.5-7
CVD TiN	4.2-4.7
PVD TiN	3.0-3.2

As may be seen from Table 1, when a very poor step coverage liner, such as PVD TiN is utilized, adequate adhesion of the W interconnects is provided without harming the contact resistance.

10 While the invention has been described with reference to preferred embodiment, it is to be understood by those skilled in the art that various modifications may be made thereto without departing from the spirit and scope of the invention, which is defined by the attended claims.